ABSTRACT OF THE DISCLOSURE

Disclosed is a circuit comprising a differential input amplifier stage, a capacitor stage, an inverter chain stage, and a biasing circuit. The inverter chain stage may be formed with or without feedback depending on whether a clock signal or data signal is to be translated using the disclosed circuit. The biasing circuit can be formed using either inverters or transmission gates. Moreover, the biasing circuit, the inverter chain stage, and the amplifier stage can be connected to a power down circuit which, when the translator is not being used, will ensure various circuitry of the translator will not consume extensive power. The inverter chain stage, biasing circuit, and capacitor stage are formed on both an upper and lower section to produce true and complementary outputs that have a consistent and equal delay from the transitions of the incoming differential input signal so as to minimize jitter and associated duty cycle of the translated output.